ABSTRACT OF THE DISCLOSURE

A macro block MB2 including a physical-layer circuit PHY for communications performs transmission and reception processing to and from a macro block MB1 at a clock frequency CF1. A test circuit TC includes a test transmission buffer TXB that stores a transmission data signal from a test input terminal TPI at a frequency CF2 that is lower than the frequency CF1, and a test reception buffer RXB that outputs a reception data signal to a test output terminal TPO at a frequency CF3 that is lower than the frequency CF1. After the transmission buffer TXB has stored the transmission data signal from the terminal TPI at the frequency CF2, it outputs the stored transmission data signal to the MB2 at the frequency CF1. After the reception buffer RXB has stored the reception data signal from the MB2 at the frequency CF1, it outputs the stored reception data signal to the terminal TPO at the frequency CF3.